IN THE CLAIMS

Please cancel claims 1-2 without prejudice or disclaimer of their underlying subject matter.

1-2. (canceled).

Please add the following new claims.

3. new) A phase-locked loop circuit for reproducing a channel clock, said phase-locked loop circuit comprising:

a channel clock generation reference signal frequency divider that divides a channel clock generation reference signal;

a switching frequency divider having a switch, a first switching frequency divider and a second switching frequency divider,

said first and second switching frequency dividers receiving a high-frequency signal,

said first switching frequency divider dividing said high-frequency signal by a first dividing ratio to generate a first divided signal,

said second switching frequency divider dividing said high-frequency signal by a second dividing ratio to generate a second divided signal,

said switch outputting said first divided signal during playback of a first recording medium and outputting said second divided signal during playback of a second recording medium; and

a phase comparator, said phase comparator receiving said divided channel clock generation reference signal and one of said first and second divided signals,

said phase comparator compares the phase of said divided channel clock generation reference signal with one of said first and second divided signals to output a phase error signal.

4. (new) A phase-locked loop circuit as claimed in claim 3, further comprising:

a low-pass filter, said low-pass filter generating a low-frequency signal having a level corresponding to said phase error signal;

a voltage controlled oscillator outputting a frequency signal, the oscillation frequency of said frequency signal being controlled by the level of said low-frequency signal; and

a high-frequency signal frequency divider generating said high-frequency signal from dividing said frequency signal by a variable,

said variable being changed such that said high-frequency signal is at a first frequency during said playback of said first recording medium and is at a second frequency during said playback of said second recording medium.

5. (new) A phase-locked loop circuit as claimed in claim 3, wherein said channel clock is in synchronism with data read from a disk-shaped recording medium driven for rotation.

6. (new) A phase-locked loop circuit as claimed in claim 3, wherein said first recording medium has a standard different than that of said second recording medium.

7. (new) A phase-locked loop circuit as claimed in claim 3, wherein said first recording medium is a first disk-shaped recording medium and said second recording medium is a second disk-shaped recording medium.